(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 452 817 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **91105804.8**

(51) Int. Cl.5: **H01L 29/10**, H01L 21/266

(22) Date of filing: **11.04.91**

(30) Priority: **20.04.90 JP 104580/90**

(43) Date of publication of application:
23.10.91 Bulletin 91/43

(84) Designated Contracting States:
DE FR GB

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(54) Semiconductor device with MOS-transistors and method of manufacturing the same.

(57) The present invention provides a semiconductor device having a well (25), formed in a semiconductor substrate by using a mask in which a mask pattern width of a portion corresponding to an opening diameter is equal to or less than twice the diffusion depth of the well layer, and a gate electrode (27) formed to have the well layer as a channel region of a MOS transistor. The well formed in this manner has a substantially semi-circular section to facilitate impurity concentration control in the substrate surface. When a plurality of types of opening patterns having small pattern widths are formed in a single mask, MOS transistors having different threshold voltages can be formed in a single process.

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The present invention relates to a semiconductor device and a method of manufacturing the same and, more particularly, to a semiconductor device and a method of manufacturing the same, which are suitably used when MOS transistors having different threshold voltages are to be obtained by a single step.

Conventionally, the threshold voltage of a MOS transistor and, more particularly, of a D-type (Depletion) transistor, is determined by the type and amount of an impurity used for the step of ion implantation in a channel, as shown in Figs. 1A to 1C. Fig. 1A shows a step of forming a gate insulating film 2 having a thickness of, e.g., 200 Å on, e.g., a p-type semiconductor substrate 1. Fig. 1B shows a step of ion implantation in a channel for controlling the threshold voltage of a MOS transistor. In Fig. 1B, phosphorus ions 3 are implanted at an acceleration energy of 70 KeV to a concentration of about 1×10^{12} cm^{-2} in order to form, e.g., a depletion-type transistor. Fig. 1C shows a step of forming a gate electrode 4 and source and drain diffusion layers 5. In this case, when n-type polysilicon is used as the material of the gate electrode 4, the threshold voltage of the transistor is about -2 V. Reference numeral 6 denotes an insulating film; and 7, an aluminum wiring layer.

In this conventional example, however, when transistors having different threshold voltages are to be formed, different types of ions must be implanted in different amounts at different places in order to set different threshold voltages. In other words, the same number of photoengraving steps as that of the required threshold voltages are required, resulting in a great increase in the number of steps. A conventional well layer is obtained by performing impurity implantation through a considerably large opening of a mask pattern (opening diameter). Therefore, the conventional well have a uniform surface impurity concentration. To form transistors having different threshold voltages in the conventional well, it is also necessary to implant different types of ions in different amounts into the different parts of the well. In this case, too, the same number of photoengraving steps as that of the threshold voltages need to be performed.

The present invention has been made in view of the above situation and has as its object to provide a semiconductor device having different threshold voltages in a plurality of MOS transistors, and a method of manufacturing the same with fewer steps than in a conventional method.

In order to achieve this object, a semiconductor device according to the present invention comprises a semiconductor substrate of one conductivity type, a MOS transistor, formed in the semiconductor substrate and having source and drain layers of a conductivity type opposite to that of the semiconductor substrate, and a well layer formed in the vicinity of a channel region of the MOS transistor to control a threshold voltage thereof, wherein the well layer has a substantially semi-circular section with a non-flat lower surface. Also, a method of the present invention comprises the steps of forming a mask in which a mask pattern width of a portion corresponding to a mask opening diameter is equal to or less than twice the diffusion depth of a well layer, and implanting an impurity in a prospective channel portion of a MOS transistor of a semiconductor substrate by using the mask, thereby forming the well layer.

More specifically, according to the present invention, there is provided a semiconductor device having a well formed in a semiconductor substrate by setting the width of a portion of a mask pattern, used for impurity implantation, that corresponds to an opening diameter to be equal to or less than twice the diffusion depth of a well layer, and gate electrodes formed to have the well layer as a channel region of a MOS transistor. The well formed in the above manner has a substantially semi-circular section to facilitate impurity concentration control in the surface of the substrate (in the conventional well, since the impurity is implanted through a portion of a mask pattern having a considerably larger width than in the present invention, the surface concentration is uniform and it is difficult to control the threshold voltage). Furthermore, since a plurality of types of opening patterns having a small mask pattern width are formed in a single mask, MOS transistors having different threshold voltages can be formed in a single process.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figs. 1A to 1C show steps of manufacturing a conventional semiconductor device;

Figs. 2A to 2E show steps of manufacturing a semiconductor device according to an embodiment of the present invention;

Fig. 3A is a graph of resist space - diffusion depth characteristics used for explaining the embodiment of the present invention, and Fig. 3B is a graph of resist space - surface impurity concentration characteristics used for explaining the embodiment of the present invention;

Fig. 4A is a plan view of a pattern of another embodiment of the present invention, and Fig. 4B is a sectional view taken along the line A - A' of Fig. 4A;

Fig. 5A is a plan view of a pattern of still another embodiment of the present invention, and

Fig. 5B is a sectional view taken along the line B - B of Fig. 5A; and

Fig. 6 is a schematic sectional view of still another embodiment of the present invention.

An embodiment of the present invention will be described with reference to Figs. 2A to 2E. First, as shown in Fig. 2A, a first thermal oxide film 22 is formed on a p-type substrate 21 having an impurity concentration of about 3×10^{15} cm^{-3}. Subsequently, a resist mask 23 having resist patterns of different opening widths (mask pattern widths) is formed on prospective depletion-type transistor regions, as shown in Fig. 2B. Phosphorus ions are implanted in the substrate 21 at a dose of about 7×10^{13} cm^{-2} and an acceleration energy of 70 KeV. The structure is then annealed at 1,150°C for about 4 hours to diffuse the phosphorus. As a result, a depth X_{j1} of a diffusion layer 24 formed by phosphorus diffusion using a resist pattern 23_1 having a large width, e.g., 8 μm, is about 3 μm. The surface phosphorus concentration is about 3×10^{17} cm^{-3}. However, a depth X_{j2} of a well 25 formed by using a resist pattern 23_2 having a small width of 1 μm becomes 1 μm, and the surface concentration thereof is about 5×10^{16} cm^{-3}.

Thereafter, the oxide film 22 is removed, and a gate insulating film 26 is deposited for about 200 Å. MOS transistor gate electrodes 27 are formed at portions corresponding to the resist patterns 23_1 and 23_2. Source and drain diffusion layers 28 are formed by, e.g., ion implantation. Then, an aluminum wiring layer 30 is formed over an insulating film 29 formed on the substrate as shown in Fig. 2E, thus completing MOS transistors.

The well 24 shown in Figs. 2C to 2E is formed using the resist pattern 23_1 having a mask width greatly larger than twice its diffusion depth x_{j1} and corresponds to a conventional well. The well 25 is formed by using the resist pattern 23_2 having a mask width equal to or less than twice its diffusion depth X_{j2}. The well 25 has a substantially semicircular section and is appropriate for threshold voltage control. This is because when a pattern opening diameter is small, the impurity concentration and the depth of a diffusion layer (especially that of an ion-implantation type) are determined by the pattern opening diameter. In this case, the length of the gate electrode on the well 25 in the channel lengthwise direction is also equal to or less than twice its well diffusion depth.

Fig. 3A shows the resist space (opening pattern width) - diffusion depth characteristics of this embodiment, and Fig. 3B shows the resist space - diffusion layer surface impurity concentration characteristics of the same. The surface impurity concentration influences the threshold voltage of the MOS transistor. As is apparent from Figs. 3A and 3B, when the opening pattern is set to have a width equal to or less than twice the diffusion depth, the surface impurity concentration is greatly reduced, and the diffusion depth becomes small. In other words, when the opening pattern width is set small, i.e., equal to or less than twice the diffusion depth, in the case of an n-channel MOS transistor, as in this embodiment, the threshold voltage can be changed in the positive direction (p-type impurity concentration is increased; n-type impurity concentration is decreased). When the pattern width becomes 0, the impurity concentration becomes identical to that of the p-type semiconductor substrate.

Fig. 4A is a plan view of a pattern according to another embodiment of the present invention, and Fig. 4B is a sectional view taken along the line A - A' of Fig. 4A. The same reference numerals as in Figs. 2A to 2E denote the same or identical portions in Figs. 4A to 4B. In this embodiment, a plurality of mask patterns 23_2 for impurity implantation are arranged on the channel regions of the MOS transistors. In this case, the diameter of each mask pattern 23_2 is equal to or less than twice its diffusion depth. More specifically, a plurality of circular resist patterns 23_2 are formed in the channel regions of, e.g., MOS transistors, as shown in Fig. 4A. Phosphorus is implanted in these regions, and diffusion is subsequently performed to appropriately set the surface phosphorus concentration. As a result, the threshold voltages of the MOS transistors can be set.

Another narrow diffusion layer pattern can be arranged to be perpendicular to the channel lengthwise direction. Fig. 5A is a plan view of a pattern of this example, and Fig. 5B is a sectional view taken along the line B - B of Fig. 5A. In this embodiment, e.g., two mask patterns 23_2 for impurity implantation are arranged parallel to the channel widthwise direction of the MOS transistors. In this case, the condition of the pattern width being equal to or less than twice the diffusion depth must apply only to the widthwise direction (shorter direction) of the mask patterns 23_2, and need not apply to the lengthwise direction.

Fig. 6 shows still another embodiment of the present invention. When the threshold voltage goes more toward the plus side than the case of Figs. 2A to 2E, a well 25 as shown in Fig. 6 may be adopted. The well 25 must similarly satisfy the above condition (the width must be equal to or less than twice the diffusion depth).

The present invention is not limited to the above embodiments but various changes and modifications can be made within the spirit and scope of the invention. For example, the shape of the mask pattern can be changed in various manners. In the above embodiments, the well is of a conductivity type opposite to that of the semiconductor substrate. However, the present invention can also be applied to an enhancement-type semi-

conductor device wherein the conductivity type of the well 25 is changed so that it will be of the same conductivity type as that of the substrate 21. In the above embodiments, the well has a "semi-circular" shape. However, it does not mean a true semi-circle but a shape whose bottom is not flat, unlike the well 24, but is curved, like the well 25.

According to the present invention, MOS transistors having different threshold voltages can be formed by the same manufacturing process (photoengraving steps) by forming a plurality of patterns having different opening diameters in a single mask, thus resulting in greatly simplified manufacturing steps.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A semiconductor device comprising a semiconductor substrate (21) of one conductivity type, a MOS transistor, formed in said semiconductor substrate and having source and drain layers (28) of a conductivity type opposite to that of said semiconductor substrate, and a well layer (25) formed in the vicinity of a channel region of said MOS transistor to control a threshold voltage thereof, wherein said well layer has a substantially semi-circular section with a non-flat lower surface.

2. A device according to claim 1, characterized in that said well layer is of the same conductivity type as that of said source and drain layers of said MOS transistor.

3. A device according to claim 1, characterized in that said well layer is of a conductivity type opposite to that of said source and drain layers of said MOS transistor.

4. A method of manufacturing a semiconductor device, comprising the steps of manufacturing a mask (23) in which a mask pattern width (23_2) of a portion corresponding to a mask opening diameter is not more than twice a diffusion depth of a well layer (25), and forming said well layer by implanting an impurity in a prospective channel region of a MOS transistor of a semiconductor substrate by using said mask.

5. A method according to claim 4, characterized in that the length of a gate electrode (27) of said MOS transistor in a channel lengthwise direction is not more than twice the diffusion depth of said well layer in the channel lengthwise direction.

6. A method according to claim 4, characterized in that a single mask has a plurality types of mask pattern widths corresponding to mask opening diameters.

7. A method according to claim 6, characterized in that the mask also includes an opening pattern (23_1) of a condition other than that for the mask pattern widths corresponding to the mask opening diameters.

8. A method according to claim 4, characterized in that said source and drain layers of said transistor are formed by ion implantation by using a gate (27) portion formed on said well layer as a mask.

9. A method according to claim 4, characterized in that a plurality of elongated mask patterns for impurity implantation are arranged parallel to the channel widthwise direction of said MOS transistor.

10. A method according to claim 4, characterized in that said plurality of mask patterns for impurity implantation are arranged on channel regions of a plurality of said MOS transistors.

11. A method according to claim 4, characterized in that said well layer is of the same conductivity type as that of said source and drain layers of said MOS transistor.

12. A method according to claim 4, characterized in that said well layer is of a conductivity type opposite to that of said source and drain layers of said MOS transistor.

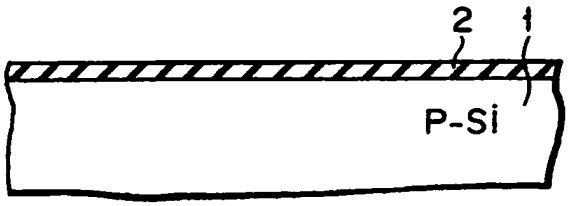


FIG. 1A

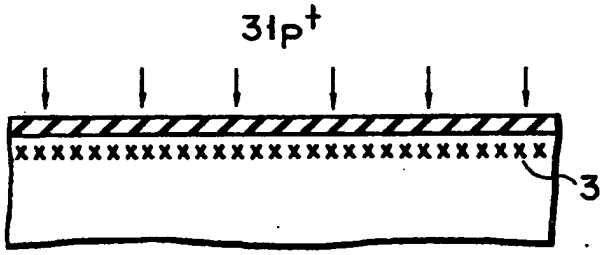


FIG. 1B

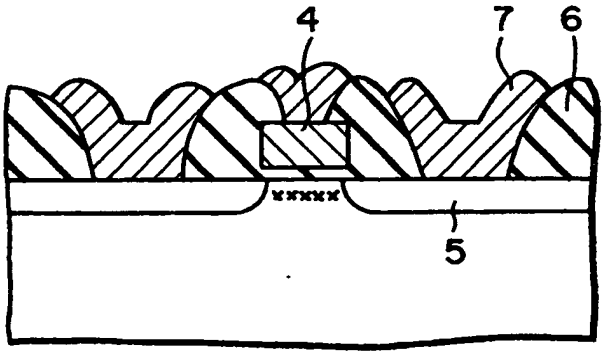


FIG. 1C

FIG. 2A

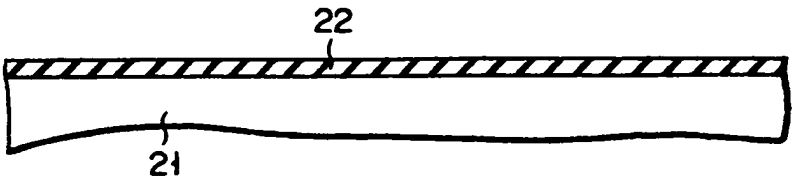


FIG. 2B

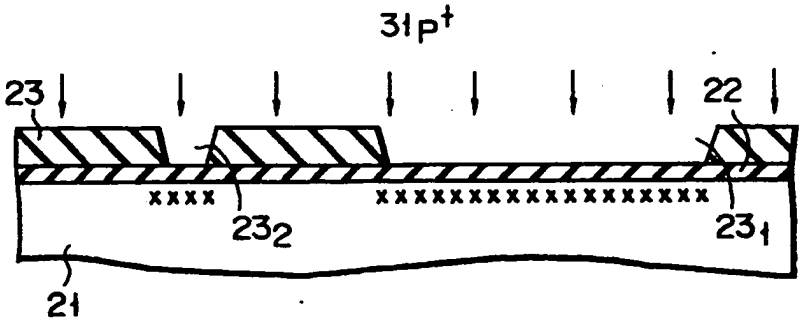


FIG. 2C

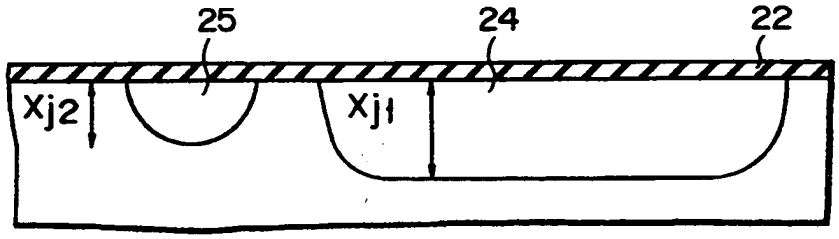


FIG. 2D

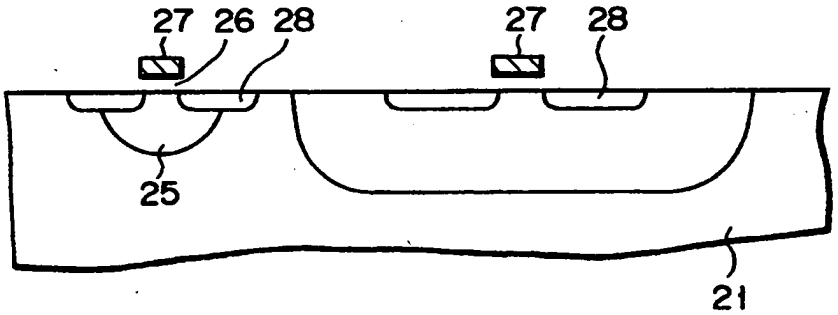
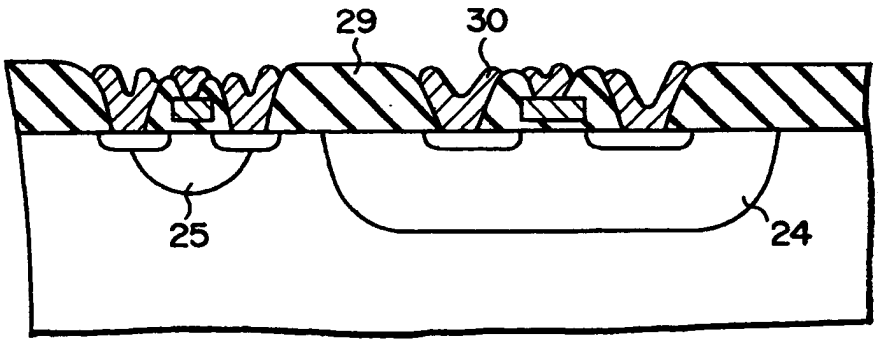


FIG. 2E



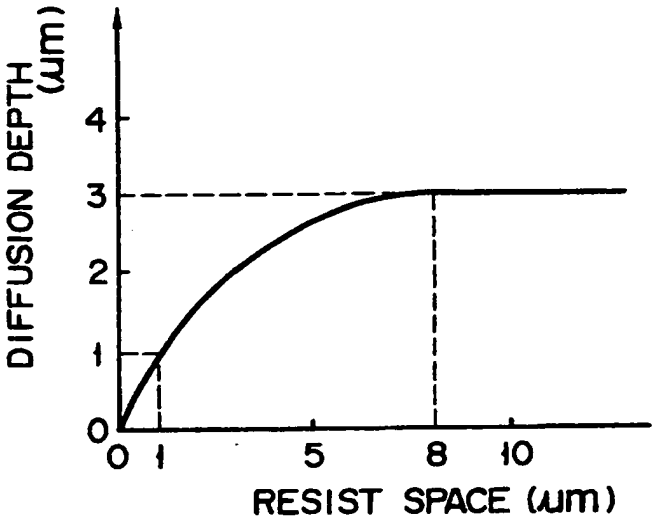

DIFFUSION DEPTH (μm)
4
3
2
1
0
0
1
5
8
10
RESIST SPACE (μm)

FIG. 3A

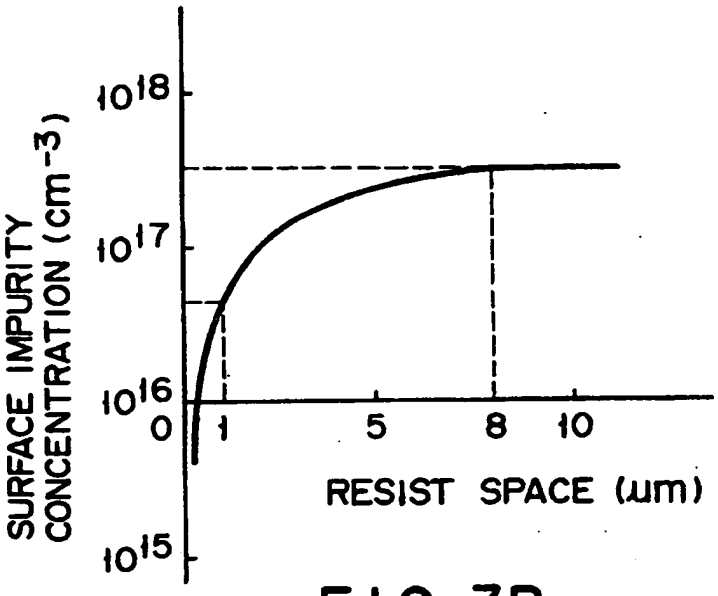

SURFACE IMPURITY CONCENTRATION (cm-3)
10^18
10^17
10^16
10^15
0
1
5
8
10
RESIST SPACE (μm)

FIG. 3B

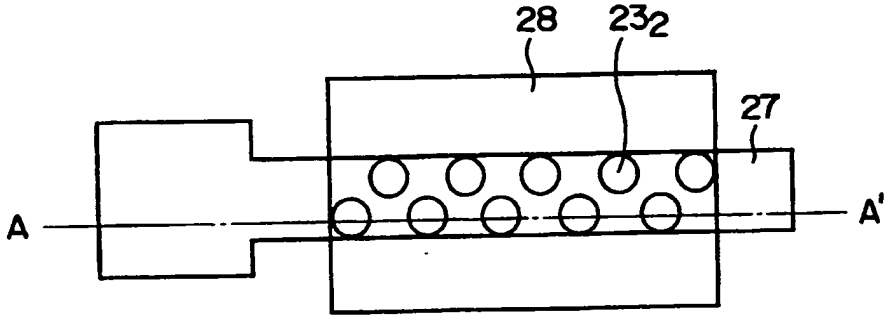


FIG. 4A

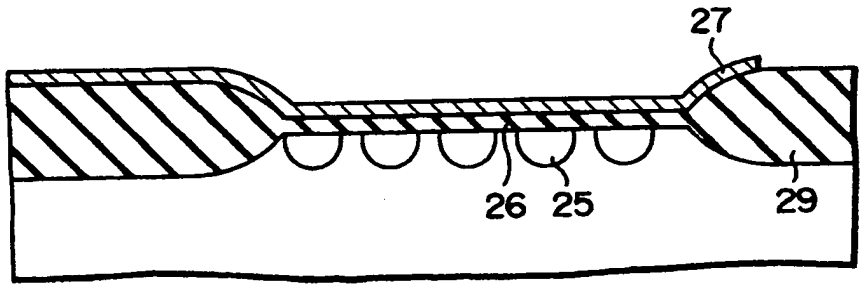


FIG. 4B

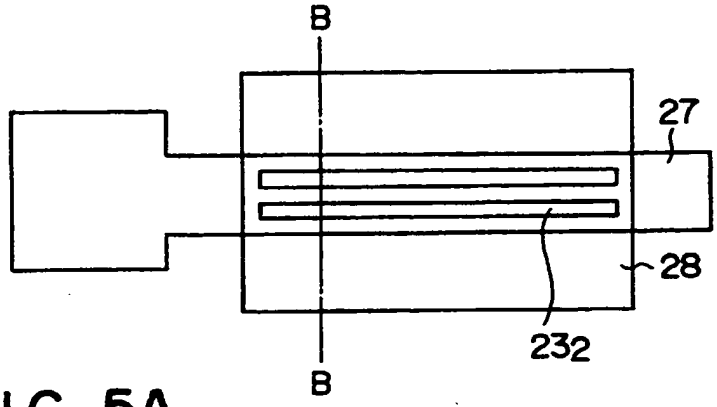


FIG. 5A

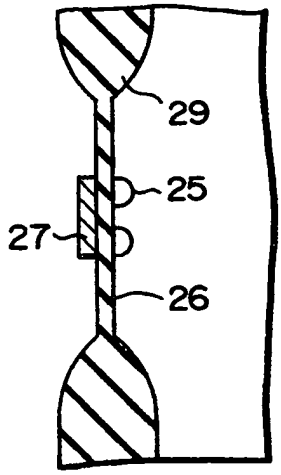


FIG. 5B

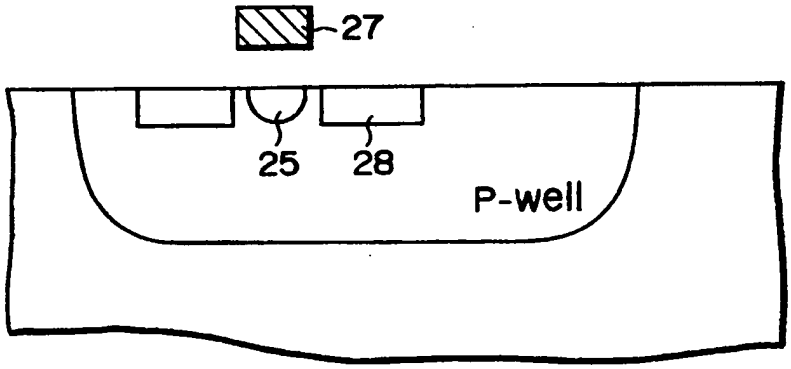


FIG. 6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 10 5804

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	PATENT ABSTRACTS OF JAPAN vol. 11, no. 174 (E-513)(2621), 4 June 1987; & JP - A - 628553 (TOSHIBA) 16.01.1987 * abstract; figure *	1-12	H 01 L 29/10 H 01 L 21/266
A	I.E.E.E. TRANSACTIONS ON ELECTRON DEVICES vol. ED-33, no. 3, March 1986, pages 426-428, New York, NY, US; R. STENGL et al.: "Variation of Lateral Doping as a Field Terminator for High-Voltage Power Devices" * page 426; figures 1-3 *	1-12	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
Berlin	08 July 91	JUHL A.

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
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